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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/982,829	10/22/2001	Yong-Suk Go	8733.080.10	8486

30827 7590 03/09/2004

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EXAMINER
KOVALICK, VINCENT E

ART UNIT	PAPER NUMBER
2673	14

DATE MAILED: 03/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/982,829	GO, YONG-SUK	
	Examiner	Art Unit	
	Vincent E Kovalick	2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 January 2004* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15 and 25-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *29-33* is/are allowed.

6)☒ Claim(s) *1-3,6-8,14 and 25-28* is/are rejected.

7)☒ Claim(s) *4,5,9-13 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This Office Action is in response to Applicant's RCE (Request for Continued Examination and Reconsideration, dated January 20, 2004.

2. The following is a response to Applicant's Remarks/Arguments.

o Applicant's arguments relative to claims 1 and 7 filed January 20, 2004 have been fully considered but they are not persuasive.

Regarding claim 1, with regard to the limitation "at lease two bit lines, each bit line transmitting a bit signal having a voltage level" Watney teaches (col. 6, lines 25-39) an input bus which is made up of at least two bit lines that carry a voltage signal. Further, Shau teaches "at lease two voltage control means connected to the corresponding bit lines, wherein each voltage control means changes the voltage level of the bit liens at a different ration from the other voltage control means", Watney (col. 28, lines 45-49) teaches voltage control means for controlling the bit-lines to have a bit line voltage higher, lower and within a medium voltage range between a first voltage and a second voltage. Further still, regarding the limitation 'adder means for adding voltage levels outputted form the two voltage control means to generate an analog signal", Kobayashi et al. (col. 13, lines 27-30) teaches an analog adder the function of which is to combine analog signals (voltages) to generate a resulting analog signal.

These three references are combined to address the limitations of claim 1.

Relative to claim 7, regarding the limitation "receiving means for receiving an analog signal formed by compressing at least n-bit data, wherein n is an integer", Furuhashi et al. teaches (col. 3, lines 10-19) receiving means for receiving an analog signal formed by

compressing at least n-bit data where in n is an integer. Further, Smeets et al. teaches (col. 12, lines 39-44) "quantizing means for quantizing the analog signal form the receiving means; and coding means connected to the quantizing means for coding the quantized analog signal to reconstruct the n-bit data".

These two references are combined to address the limitations of claim 7.

Applicant's arguments relative to claims 25-33 are rendered moot in light of the new action regarading said claims 25-33.

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claim 25 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 25 makes reference to n voltage converters, this limitation is not addressed in the specification.

Claims 26-28 are rejected in that they are dependent on rejected independent claim 25.

Drawing Objection

5. The drawings are objected to because they do not show the *voltage converters* taught in claim 25. A proposed drawing correction or corrected drawings are required in reply to the

Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Watney (USP 5,930,398) taken with Shau (USP 404,670) in view of Kobayashi et al (USP 4,859,871).
Relative to claim 1, Watney **teaches** a method and apparatus for determining a quantizing factor for multi-generation data compression/decompression processes (col. 3, lines 22-67; col. 4, lines 1-67 and col. 5, lines 1-16). Watney further **teaches** a bus compressing apparatus comprising at least two bit lines, each bit line transmitting a bit signal having a voltage level (col. 6, lines 25-39 and Fig. 2). It being understood that data transmission means include data (bit) lines and that the data is represented by voltage levels.
Watney **does not teach** at least two voltage control means (voltage converters) connected to the corresponding bit lines, wherein each voltage control means changes the voltage level of the bit line at a different ratio from the other voltage control means; or adder means for adding voltage levels outputted form the two voltage control means to generate an analog signal.
Watney teaches data compression and decompression processes and method thereof.
Shau **teaches** devices having first level bit lines connected along different layout directions (col. 4, lines 1-67; col. 5, lines 1-11). Shau further **teaches** at least two voltage control means (voltage converters) connected to the corresponding bit lines, wherein each voltage control

means changes the voltage level of the bit line at a different ratio from the other voltage control means (col. 28, line 43-47).

Watney taken with Shau **does not teach** adder means for adding voltage levels outputted form the two voltage control means to generate an analog signal.

Watney taken with Shau teaches data compression and decompression processes and method thereof, with voltage control means for controlling bitlines having variable voltages.

Kobayashi et al. **teaches** a voltage level setting circuit (col. 2, lines 61-68 and col. 3, lines 1-36).

Kobayashi et al. further **teaches** adder means for adding voltage levels outputted form the two voltage control means to generate an analog signal (col. 13, lines 27-30).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to incorporate in the device as taught by Watney the features as taught by Shau in view of Kobayashi et al. in order to include in the system those features necessary to transmit the bit data being input to the at least two voltage converter and in turn generate an analog signal.

Regarding claim 6, Kobayashi et al. **teaches** a bus compression apparatus wherein the adder means performs a wired sum operation (col. 13, lines 27-30). It being understood that the means for, and concept of, wired summing is in common practice in the art.

8. Claims 2-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watney taken with Shau in view of Kobayashi et al. as applied to claim 1 in item 7 hereinabove, and further in view of Ng et al. (USP 5,847,616).

Regarding claims 2-3 Watney taken with Shau in view of Kobayashi et al. **does not teach** said bus compressing apparatus wherein the two voltage control means includes a first voltage control means comprising a first resistor and a second voltage control means comprising a second resistor; and wherein the first resistor and the second resistor have different resistance.

Watney taken with Shau in view of Kobayashi et al. teaches data compression and decompression processes and method thereof, with voltage control means for controlling bitlines

having variable voltages, with adder means for adding voltage levels for generating an analog signal.

Ng et al. **teaches** an embedded voltage controlled oscillator with minimum sensitivity to process and supply (col. 2, lines 31-64). Ng et al. further **teaches** two voltage control means includes a first voltage control means comprising a first resistor and a second voltage control means comprising a second resistor; and wherein the first resistor and the second resistor have different resistance (col. 7, lines 29-38).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to incorporate in the device as taught by Watney taken with Shau in view of Kobayashi et al. the feature as taught by Ng et al. in order to provide the first and second voltage control means with circuit structure that would facilitate changing the voltage level of the bit line of a first voltage control at a different ratio from a second voltage control means.

9. Claims 7 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Furuhashi et al. (USP 5,850,540) taken with Smeets et al. (USP 6,218,968) in view of Taguchi (USP 5,815,080).

Relative to claims 7 and 14, Furuhashi et al. **teaches** a method and apparatus for timesharing CPU system bus in an image generation system (col. 3, lines 64-67; col. 3, lines 1-67; col. 4, lines 1-67 and col. 5, lines 1-53). Furuhashi et al. further **teaches** a bus decompressing apparatus compressing: receiving means for receiving an analog signal formed by compressing at least n-bit data, wherein n is an integer (col. 2, lines 46-54 and col. 3, lines 9-18 and 41-56). Furuhashi et al. **does not teach** quantizing means for quantizing the analog signal from the receiving means; and coding means connected to the quantizing means for coding the quantized analog signal to reconstruct the n-bit data; or a plurality of level detectors parallely connected to the input line to output a quantized signal.

Furuhashi et al. teaches receiving means for receiving a compressed analog signal.

Smeets et al. **teaches** a method for encoding data (col. col. 1, lines 42-67 and col. 2, lines 1-59). Smeets et al. further **teaches** quantizing means for quantizing the analog signal from the receiving means; and coding means connected to the quantizing means for coding the quantized analog signal to reconstruct the n-bit data (col. 12, lines 41-44).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to incorporate in the devices of Furuhashi et al. the features as taught by Smeets et al in order to put in place the means necessary to decompress compressed data and reconstruct the signal being processed for presentation to a display device.

10. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Furuhashi et al. taken with Smeets et al. as applied to claims 7 in item 9 hereinabove, and further in view of Kondo (USP 6,222,398).

Relative to claims 8, Furuhashi et al. taken with Smeets et al. **does not teach** a bus decompressing apparatus wherein quantizing means includes at least (2 *to the* n *power* - 1) level detectors connected in parallel between the receiving means and the coding means, each level detector being configured to detect different voltage levels of the analog signal.

Furuhashi et al. taken with Smeets et al. teaches receiving means for receiving a compressed analog signal and quantizing means for quantizing the analog signal for further processing.

Kondo **teaches** a voltage detection circuit (col. 2, lines 43-56). Kondo further **teaches** quantizing means includes at least (2 *to the* n *power* - 1) level detectors connected in parallel between the receiving means and the coding means, each level detector being configured to detect different voltage levels of the analog signal (col. 2, lines 43-56).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to incorporate in the device as taught by Furuhashi et al. taken with Smeets the feature as taught by Kondo in order to put in place the circuitry necessary to detect the various voltage levels associated with the compressed analog signal.

Allowable Subject Matter

11. Claims 4-5, 9-13 and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Relative to claim 4, the prior art of record **does not teach** a bus compressing apparatus wherein the resistance value of the second resistor of the second voltage control means is ½ *to the* n *power* of the resistance value of the first resistor, in which n is an integer.

Regarding claim 5, the prior art of record **does not teach** a bus compressing apparatus wherein the resistance value of the second resistor of the second voltage control means is ½ of the resistance value of the first resistor.

Relative to claim 9 the prior art of record **does not teach** a bus decompressing apparatus wherein each one of the level detectors comprises: a transistor controlled by the analog signal from the receiving means; and output voltage control means connected to the transistor to output the quantized analog signal to the coding means in response to the analog signal.

Regarding claim 13, the prior art of record **does not teach** a bus decompressing apparatus wherein the quantizing means includes first, second and third level detectors, each level detector having a transistor with a threshold voltage, the transistor being connected between a first voltage and a second voltage, wherein the transistor of the first level detector turns on when the analog signal is above the second voltage, the transistor of the second level detector turns on when the analog signal is above the second voltage by about 1/3 of the difference between the first and second voltages, and the transistor of the third level detector turns on when the analog signal is above the second voltage by about 2/3 of the difference between the first and second voltage.

12. Claims 29-33 are allowed.

13. The following is an examiner's statement of reasons for allowance:

Relative to claim 29, the major difference between the teachings of the prior art of record (Watney, Furuhashi et al. and Smeets et al.)and that of the instant invention is that said prior art of record **does not teach** a bus decompressing apparatus comprising a coding device connected to a plurality of level detectors to code quantized signals to reconstruct an n-bit data.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U. S. Patent No.	6,064,771	Migdal et al.
U. S. Patent No.	5,883,925	Sinibaldi et al.
U. S. Patent No.	4,951,139	Hamnilton et al.

Responses

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent E Kovalick whose telephone number is 703 306-3020. The examiner can normally be reached on Monday-Thursday 7:30- 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 703 305-4938. The fax phone numbers for the organization where this application or proceeding is assigned are 703 872-9314 for regular communications and 703 872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 306-0377.

Vincent E. Kovalick

March 8, 2004

BIPIN SHALWALA
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